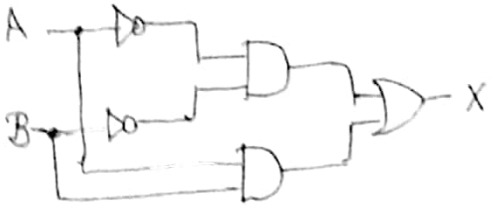
VSSC 06 08 2017
T 2H MaxM:320
No. of Q 80
Version A

ED - 2	OFC -		MP 8085 - 8
AEC - 12	MC - 1		MP 8086 - 6
DE - 18	RC - 5		MC 8051 -
AC - 11	AWG - 4		LIC - 4
DC - 05	EMT - 2		NLB - 2
TL - 5	TV -		NLB(TS) -
Maths - 6	MBI		EE

(1) (B) What type of logic circuit is represented by the figure shown below?



(a) XOR (b) XNOR (c) AND (d) NAND

Sol: $\bar{A}\bar{B} + AB = X$ (ANS)

(2) (A) To address a memory location out of N memory locations, the no. of address lines required is

(a) log N (to the base 2) (b) log N (to the base 10) (c) log N (to the base e)

(d) log (2N) (to the base e)

$2^{16} = 65,536 \Rightarrow 2^n = N$

$\log_2 N = \frac{\log_{10} N}{\log_{10} 2} = \frac{\log_{10} 65,536}{\log_{10} 2} = 16$

(11) (B) The o/p of a logic gate is 1 when all its i/p's are logic 0. The gate is either (a) NAND or Ex-OR gate (b) NOR or Ex-NOR gate (c) OR or Ex-OR gate (d) AND or Ex-OR gate.

NOR

0	0	1
0	1	0
1	0	0
1	1	0

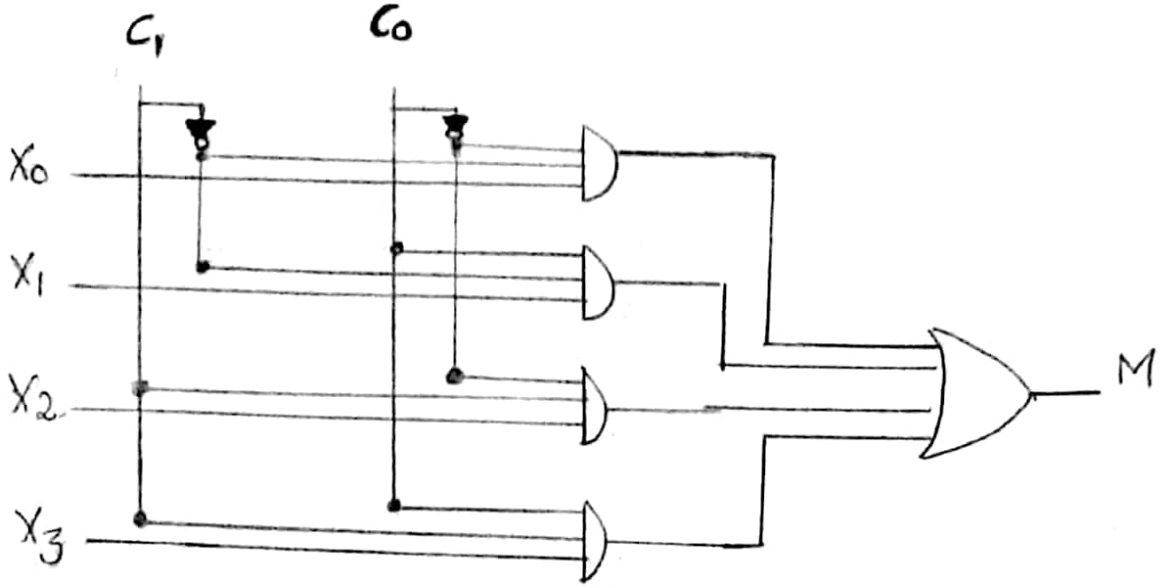
EX NOR

0	0	1
0	1	0
1	0	0
1	1	1

(18) (B) In the given 4-to-1 multiplexer, if C1=0 & C0=1 then O/P is

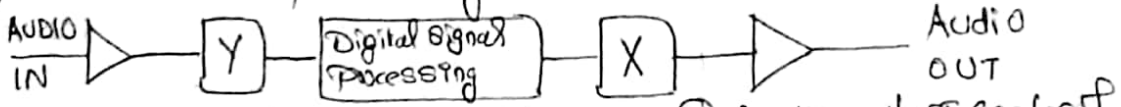
(a) X0 (b) X1 (c) X2 (d) X3.

B



(19)

(23) (B) What function is performed by the block labelled X in the given figure?



(a) ADC (b) DAC (c) Audio ON/OFF Control (d) Power supply for the audo amplifier.

(24) (D) What is the max Conversion time for an 8 bit SAC ADC with a CLK freq of 20kHz?

(a) 12.8 mS (b) 6.4 mS (c) 0.05 mS (d) 0.4 mS

for SAC ADC, processing of each bit takes one CLK cycle

N bit SAC ADC will have a total Conversion time N CLK cycles

t_C for SAC = (N x 1) CLK cycles.

Here Conversion time = 8 CLK period $= 8 \times \frac{1}{20kHz} = 0.4 \times 10^{-4} = \frac{4}{10} \times 10^{-3}$

1 CLK period $= \frac{1}{20kHz}$

$= 0.4$ mS (ANS)

(33) (B) If the range of output voltage of a 6 bit DAC is 0 to 15 volts, what is the step voltage of the o/p.

(a) 0.117 volt/step (b) 0.234 volt/step (c) 2.13 volts/step (d) 4.26 volts/step.

for N bit DAC, no of different levels $= 2^N$

No of steps $= 2^N - 1$

As N inc: no of steps ↑, step size ↓, resolution ↓

$N = 6$

no of steps $= 2^N - 1 = 63$

FSO $= 15$ V

FSO = no of steps × step size

Step size $= \frac{15}{63} = 0.238$ V/steps

(ANS)

(34) (C) Given that $16_{10} = 100_x$. Find the value of x

(a) 2 (b) 3 (c) 4 (d) 16.

$16_{10} = 100_x$

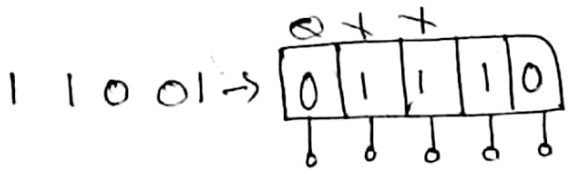
$1 \times 10^2 + 6 \times 10^0 = 1 \times x^2 + 0 \times x^1 + 0 \times x^0$

$10 + 6 = x^2 \Rightarrow x = \pm 4$ (ANS)

(43)

(44) (C) The group of bits 11001 is serially shifted (right-most bit first) into a 5 bit parallel o/p shift register with an initial state 01110. After 3 clk pulses, the register contains —

(a) 01110 (b) 00001 (c) 00101 (d) 00110



1st clk	1	0	1	1	1
2nd clk	0	1	0	1	1
3rd clk	0	0	1	0	1

(ANS)

(56) (C) The terminal count of a typical modulus-10 binary counter is

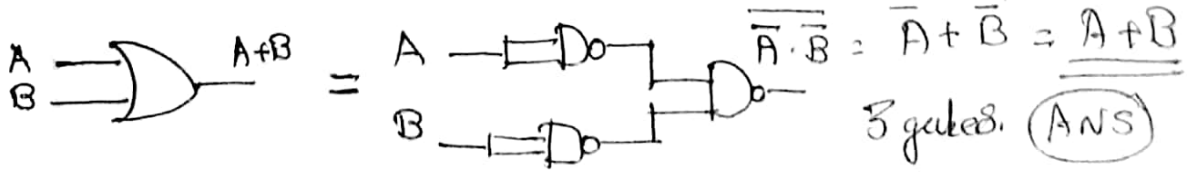
(a) 0000 (b) 1010 (c) 1001 (d) 1111

terminal count is the last count in a cycle

mod 10 counts 0 thru 9 → 0 thru 9 ---- ∴ 1001 (ANS)

(57) (B) What is the minimum no. of two i/p NAND gates need to perform the function of two i/p OR gate?

(a) 2 (b) 3 (c) 4 (d) 6



3 gates. (ANS)

(19) (A) Which Stmt is true regarding Asynchronous Counters?

(a) LF applications are limited because of internal propagation delays.

(b) HF applications are limited because of internal propagation delays.

(c) Asyn. Counters do not have major drawbacks & are suitable for use in high & LF Counting applications.

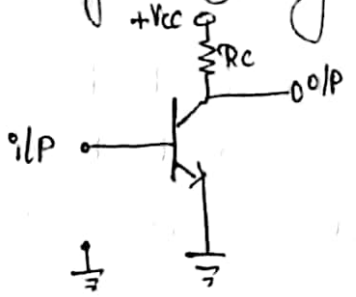
(d) Asyn. Counters do not have propagation delays, which limits their use in HF applications.

if T_c → period of CLK pulse
n → no. of Stages
t_{pd} → prop delay in each Stage
f_c → CLK frequency

$\frac{1}{T_c} = f_c < \frac{1}{n t_{pd}}$, to avoid Skipping of States.

if prop delay is large & CLK freq high (CLK period low) then Skipping may occur.

(43) (C) A Single transistor can be used to build which of the following digital logic gates? (a) AND gates (b) OR gates (c) NOT gates (d) NAND gates



I/P	O/P
L	H
H	L

(45) (B) If the memory chip size is 1024 × 4 bits, how many chips are required to make 4K bytes of memory?

(a) 4 (b) 8 (c) 16 (d) 4096

Given mem chip size 1024 × 4 bits
to make 4K bytes of memory ie 4096 × 4 bits = 4 chips (1 mark)

Since 4K bytes. 8 chips

(48) (C) No of 3 line to 8 line decoders req to select 1 out of 64 i/p's is

(a) 4 (b) 8 (c) 9 (d) 16